

A Dielectric-Defined Process for the Formation of T-Gate Field-Effect Transistors

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A novel process for the fabrication of Tee- or Gamma-shaped gate structures is presented. This process was utilized to fabricate $0.25\text{ }\mu\text{m} \times 60\mu\text{m}$ and $0.25\text{ Km} \times 150\text{ Km}$ T-gate MESFET's. From s-parameter data up to 40 GHz, extrapolated cut-off frequencies ($f_{\text{sub } t}$), as high as 55-65 GHz were obtained. This represents some of the highest $f_{\text{sub } t}$'s ever reported for a MESFET. DC yields as high as 80% over 3" wafers, were obtained using this dielectric defined T-gate (DDTG) process. Further, step-stress measurements indicate device reliability comparable to our normal MESFET process. Relative to multilayer resist processing techniques usually employed to form T-gates, we believe the DDTG process will substantially increase the yield, uniformity and reliability of FET-like devices/circuits employing T-gates with geometries at or below $0.25\text{ }\mu\text{m}$.

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